High PSRR Gain-Boosted Rail-To-Rail OTA

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Abstract - High-gain and high frequency band width operational transconductance amplifier (OTA) with high PSRR is presented in this paper which can be used in switched capacitor filters and/or pipeline A/D converters. It is demonstrated the best trade-off between DC gain, speed, and PSRR for this design. The OTA achieves a constant large signal DC gain of > 90 dB and PSRR of > -23 dB over process and temperature variations. It is designed in a 28nm CMOS process and draws a DC power of 7 mW from a 1.8-V supply. The settling time to < 0.05% accuracy for the worst case is ~ 8.3 ns. The presented correction technique can be used in the high speed ADCs and in special input/output circuits of several standards such as Peripheral Component Interconnect (PCI), Universal Serial Bus (USB) and etc.

Keywords - Power Supply Rejection Ratio (PSRR), on trans-conductance amplifier (OTA), rail-to-rail (R2R), gain-boosted, bandwidth (BW)

I. INTRODUCTION

Typical gain-boosting structures are shown in Fig. 1 Designing analog functional blocks with high gain, large bandwidth and high PSRR under limited supply voltage (0.8-1.8V) becomes more and more difficult, because when mosFETs were cascoding for PSRR improvement as a result the output signal swing becomes more and more limited. Power noise can significantly decrease performance by reducing the dynamic range of the whole system, especially in high precision systems or if the circuits that are sensitive to supply noise are at the very beginning of the power supply/reference chain. Cascoding technique is the mostly used method to achieve high gain and to reject channel length modulation effect compared to 2-stage OpAmp designs because of its superior frequency response.

In this paper presented a CMOS single supply operational transconductance amplifier (OTA) with high PSRR. A high output impedance current source and noise reduction techniques are used to improve the PSRR both at DC and at higher frequency up to the gain bandwidth (GBW) of the OTA.

Main problems while trying to cascode more transistors is a limited supply voltage. Gain-boosting technique (Fig. 1) [1] was introduced to remedy this problem. It allows increasing the DC gain of the operational amplifier without sacrificing the output swing of a regular cascade structure.

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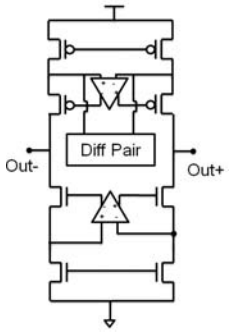


Fig.1. Gain-Boosting Technique

This can provide high speed and high gain at the same time. Gain-boosted OTA (GB OTA) [2] can have the high gain and can hold in working conditions at high speed systems such as switched capacitor filters (Fig. 2) and ADCs. It will cause to high quality performance and excluded input signals inequality. As a result of the mentioned phenomena, the system may fail to function under some operating conditions such as high temperatures or over-voltages.

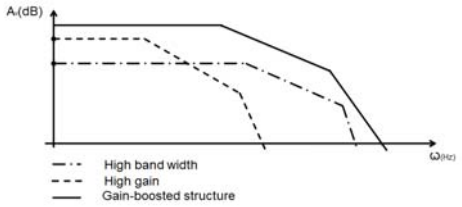


Fig.2. Bode plot for high band width, high gain and Gain-Boosting Technique

Generaly PSRR is defined as the gain from the input to the output divided by the gain from the supply to the output (Eq. (1)). At low frequencies:

$$PSRR \sim g_{mIN}\,(r_{0CSload} \| r_{0IN}) \qquad (1)$$

Where g_{mIN} is amplifier input pair condactivity, $r_{0CSload}$ and r_{0IN} are current source load and input pair channel length modulation resistance.

It needs to be pointed out that it is well known that a pole-zero doublets is often associated with gain boosting. Later in simulations results part will be present the result from a small-signal analysis of the gain-boosting technique. It will become

clear that the pole-zero doublets and its consequence (slow settling) (Fig.3.) can be very well suppressed.

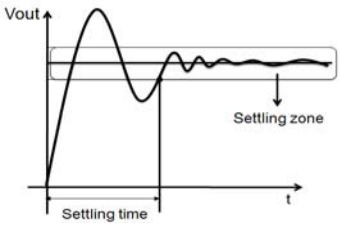


Fig.3. Settling time calculation

II. HIGH PSRR GAIN-BOOSTED OTA CIRCUIT ARCHITECTURE

The structure of proposed High PSRR GB OTA with Rail-to-Rail inputs is presented in Fig. 4.

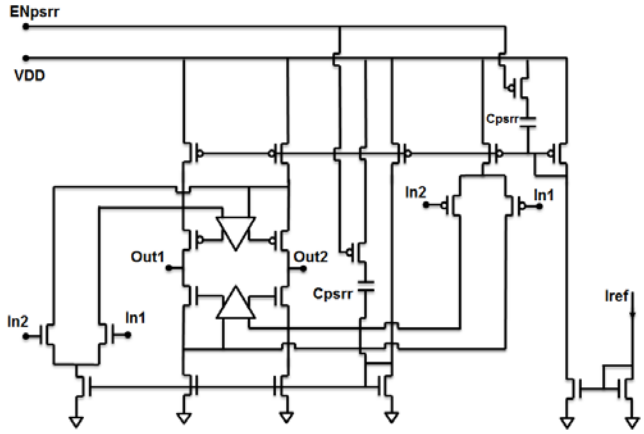


Fig.4. Circuit structure GB High PSRR OTA with Rail-to-Rail inputs

For increasing PSRR in this architecture proposed Cpsrr capacitors from supply to current mirror's bias points which can controlled by ENpsrr signal (Fig. 4.) and for input signal range proposed to use rail-to-rail method. This structure provided high small-signal gain and high PSRR with no frequency band width degradation. Therefore, optimizing the unity-gain bandwidth of the gain booster becomes difficult. A technique used in this paper is to place a small capacitor (usually a MOS cap.) from the VDD to current mirror bias points to reject noises coming from supply.

For minimizing feed forward zero effect capacitive f/b networks provides a feed forward path for input signal to bypass the OTA. Since the f/b is negative, an instant input jump introduces a big spike at the output which is, unfortunately, to the opposite side of the final output voltage. A straightforward calculation yields the following expression for this spike:

$$\Delta V_o = V_o \cdot \beta \cdot \frac{C_f}{C_f + C_L} \qquad (2)$$

Since the f/b factor is largely fixed by the closed-loop gain, the only parameter we have control on to minimize the initial spike is the ratio C_L/C_f.

In the ideal OTA, the output current is a linear function of the differential input voltage, calculated as follows:

$$I_{\text{out}} = (V_{\text{in}+} - V_{\text{in}-}) \cdot g_{\text{m}} \qquad (3)$$

where Vin+ is the voltage at the non-inverting input, Vin− is the voltage at the inverting input and g_m is the transconductance of the amplifier.

When ENpsrr signal equal to logic "0" pmos switches turning on and Cpsrr connecting corresponding current mirrors bias points to VDD and rejecting noises coming from supply.

III. OPERATION PRINCIPLE AND AMPLIFYING

Block diagram on Fig 5. has been proposed to amplifying differential signals and having high frequency bandwidth and high PSRR. As it is known the DC gain value of amplifier is reverse proportional to bandwidth. Thus it is imperative to have high DC gain and high PSRR, in order to avoid unequal distribution when the system is in the negative feedback condition. As input of OTA (Fig 5.) to rail-to-rail input stage coming differential analog signals. Then this signals providing branch current of differential amplifier and gain boosted system providing low transconductance variation. The high PSRR system which canceling power noise and OTA biasing point's voltage dependency and when ENpsrr enabling signal equal to logic "0" the system providing high PSRR output signal.

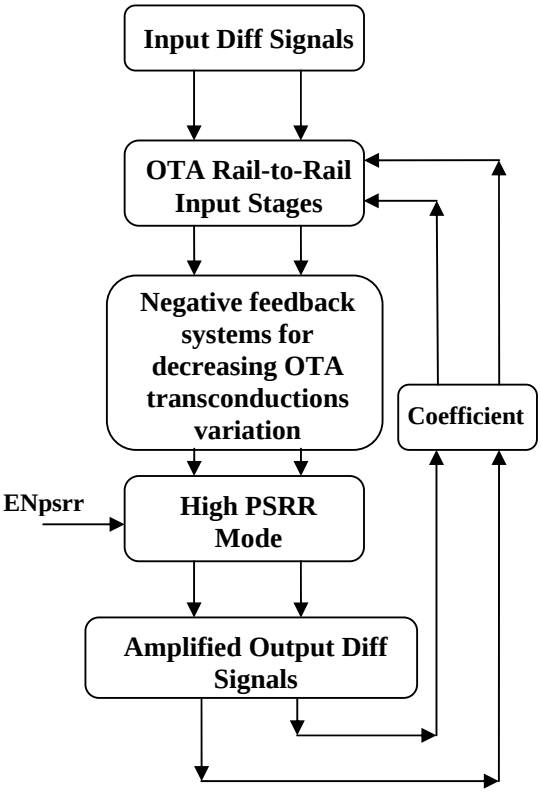


Fig.5. Block diagram of proposed method with negative feedback

As it was mentioned above the high PSRR mode enabled with ENpsrr input active signal and providing in the output high supply noise rejection over PVT.

IV. Simulation Results

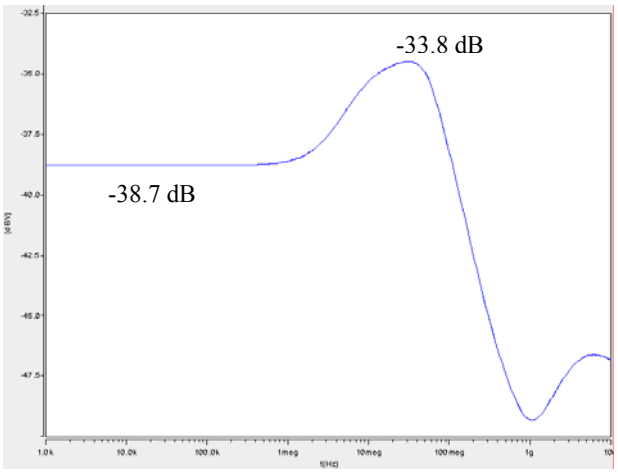
Simulations have been performed using circuit level simulator HSpice[4] for 20 PVT corners, including SS (slow-slow), TT (typical-typical), FF (fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations to estimate PSRR, small-signal gain and the unity-gain BW.

Fig. 7(a) shows OTA alternating current analyses results for TT (55^{O}) typical corner. It is seen that amplifier's max PSRR is near to -39 dB and worst PSRR is -34 dB. Fig. 7(b) and Fig. 7(c) show simulation results for, respectively, FF (-40^{O}) and SS (125^{O}) main PVT corners. Taking into consideration that USB3 protocol works with the 5Gb/s data rate signal, which means that Data have 400ps pulse period and 200ps pulse width, we have put internal specification for UGBW, PSRR and etc. After enabling PSRR mode it's changed from -15dB to -38.7dB at TT corner. In USB3 specification book phase margin min value defined as 45^{o}.

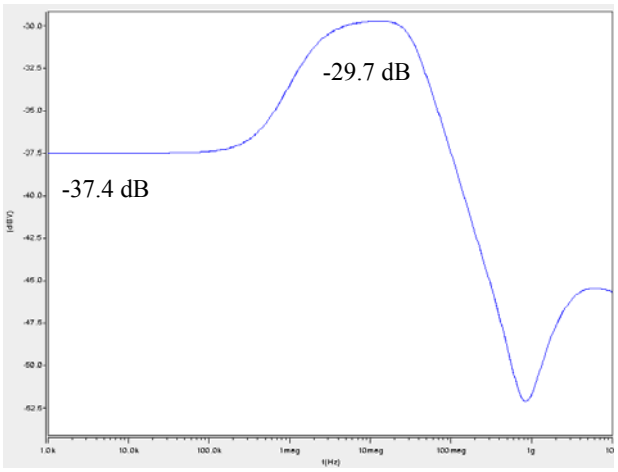
The next important parameter is Settling time (ST), which shows the time when OTA outputs is in settling zone. Table 1 shows results for 3 main corners.

TABLE I. Simulation Results of the Three Main Corners

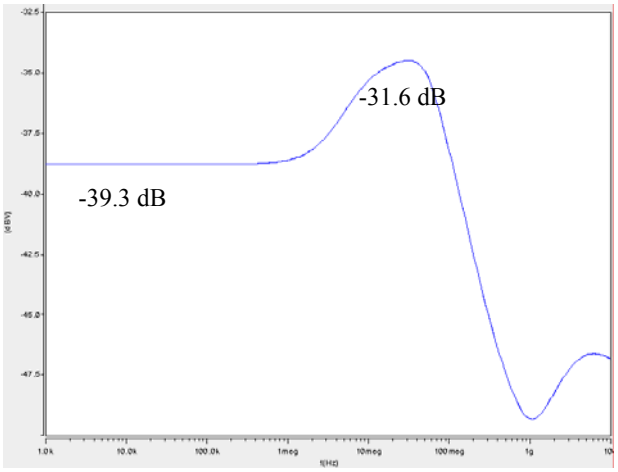
Main Parameters	Bound Corners		
	TT, 25ºC	SS, 125ºC	FF, -40ºC
Diff. Output Voltage Swing (peak-to-peak)	1.8 V		
RMS Output Noise (1 Hz to 100 GHz)	34.2µV	45.4 µV	32.7 µV
mall-Signal A_V *(gain)*	98.4 dB	96.5 dB	101.2 dB
Phase Margin (PM)	82.0 º	85.2 º	83.8 º
Unity-Gain BW	92.0 MHz	85.3 MHz	102.7 MHz
Settling Time	7.1 ns	5.3 ns	3.4 ns
Total Power Consumption	3.05 mW	3.54 mW	3.13 mW
PSRR	-38.7 dB	-37.4 dB	-39.3 dB
Worst PSRR	-33.8 dB	-29.7 dB	-31.6 dB



TT (a)



FF (b)



SS (c)

Fig.7. *OTA PSRR alternating current analyses results for TT (a), FF (b) and SS (c) corners*

VI. CONCLUSIONS

A circuit designed for high speed systems integrated in negative feedback structures. Amplifiers like proposed provided high gain, high working frequency and high PSRR from supply and ground parallelly and can operate in some settling systems as stable amplifier.

Worst PSRR value for TT corner is equal to -33.8dB and max value of PSRR is -38.7dB which without PSRR mode enabling is -15dB; the BW has the value of 92MHz and PM equal to 82^0 whereas the spec from the USB3 specification book is 45^0.

The approached method can be implemented for input/output protocols such as USB, PCI and etc.

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